Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

GENERAL DESCRIPTION

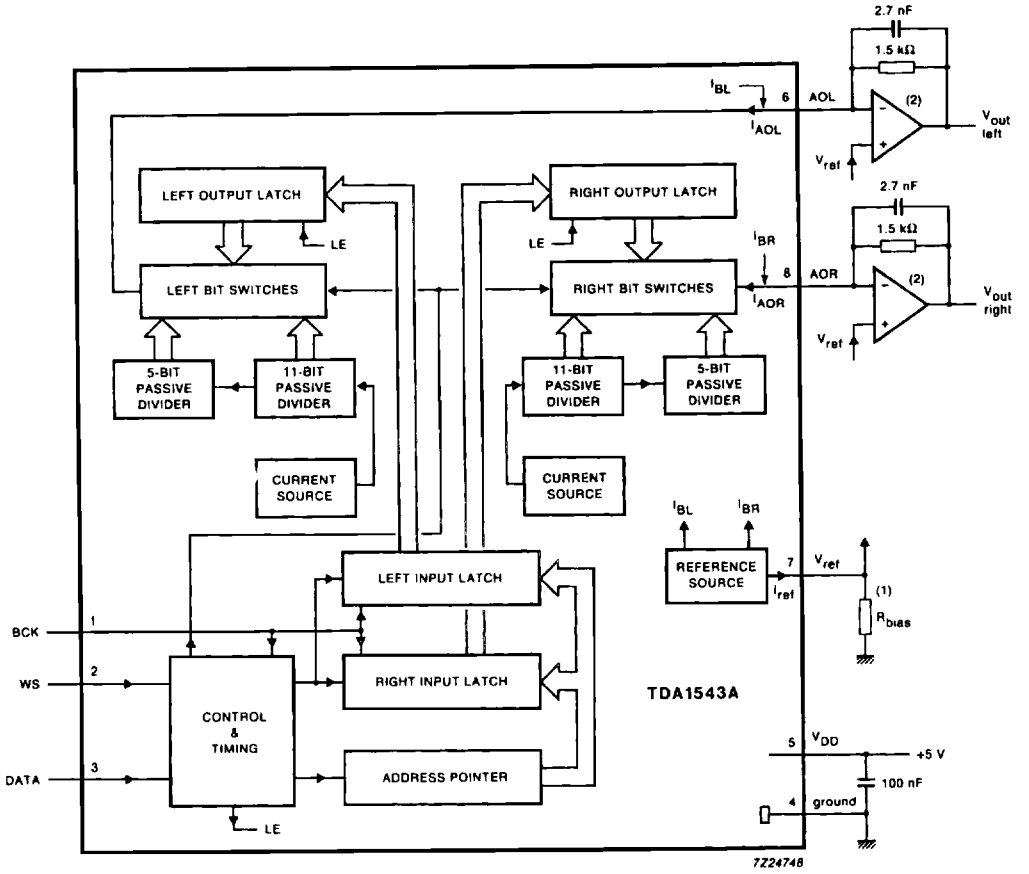
The TDA1543A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in television systems and digital amplifiers.

Features

- Low distortion
- High dynamic range
- 16-bit resolution
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese-input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Total harmonic distortion (including noise)	(D + N)/S	–	–75	–70	dB
		–	0.018	0.032	%
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	9.2	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	9.2	MHz
Signal-to-noise ratio at bipolar zero	S/N	90	95	–	dB
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.6	–	5.0	mA



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig.1 Block diagram.

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

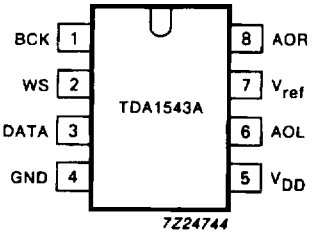
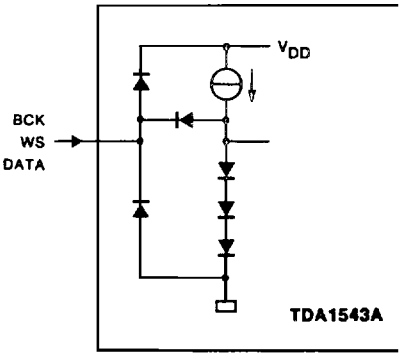
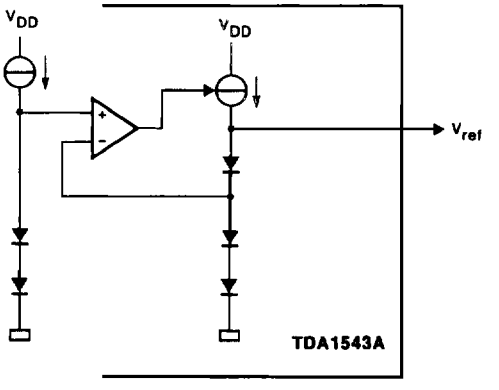


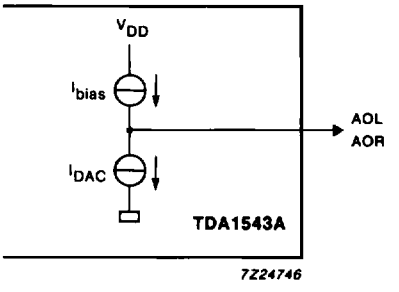
Fig.2 Pinning diagram.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	50	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	9.2	MHz
bit rate data input pin 3		BR	–	–	9.2	Mbits/s
word select input pin 2		f_{WS}	–	–	192	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.95	2.3	2.65	mA
Full scale temperature coefficient		TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Offset current	I_{ref} = 0 mA; $V_{AO} = V_{ref}$	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.6	–	5.0	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	2.1	2.2	2.3	V
Reference current output		I_{ref}	−0.3	−	2.5	mA
Total harmonic distortion (including noise)	note 3	(D + N)/S	−	−75	−70	dB
			−	0.018	0.032	%
Settling time ± 1 LSB		t_{cs}	−	0.5	−	μs
Channel separation		α	84	90	−	dB
Unbalance between outputs	note 3	$\lvert d_{IO} \rvert$	−	< 0.2	0.3	dB
Time delay between outputs		t_d	−	< 0.2	−	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	−	dB
Timing	Fig.4					
Rise time		t_r	−	−	32	ns
Fall time		t_f	−	−	32	ns
Bit clock cycle time		t_{CY}	108	−	−	ns
Bit clock HIGH time		t_{HB}	22	−	−	ns
Bit clock LOW time		t_{LB}	22	−	−	ns
Data set-up time		$t_{SU;DAT}$	32	−	−	ns
Data hold time to bit clock		$t_{HD;DAT}$	2	−	−	ns
Word select hold time		$t_{HD;WS}$	2	−	−	ns
Word select set-up time		$t_{SU;WS}$	32	−	−	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

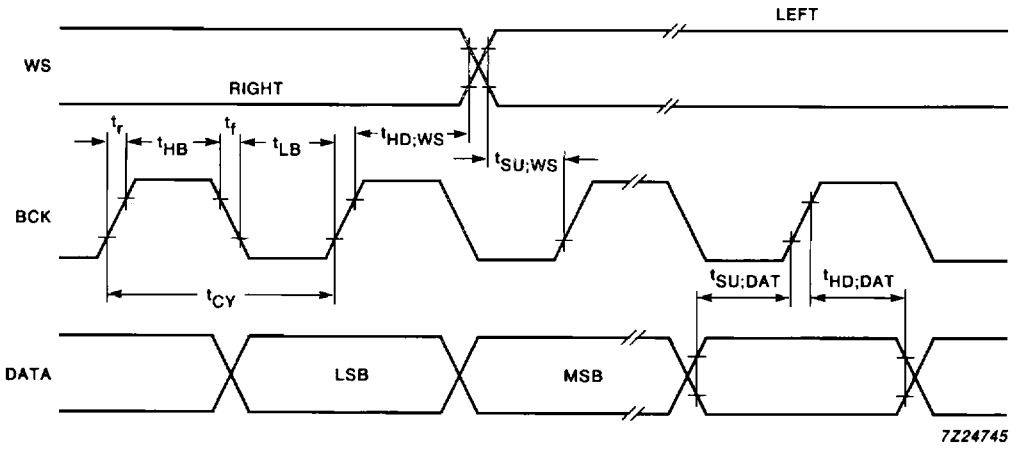


Fig.4 Format of input signals (Japanse format).

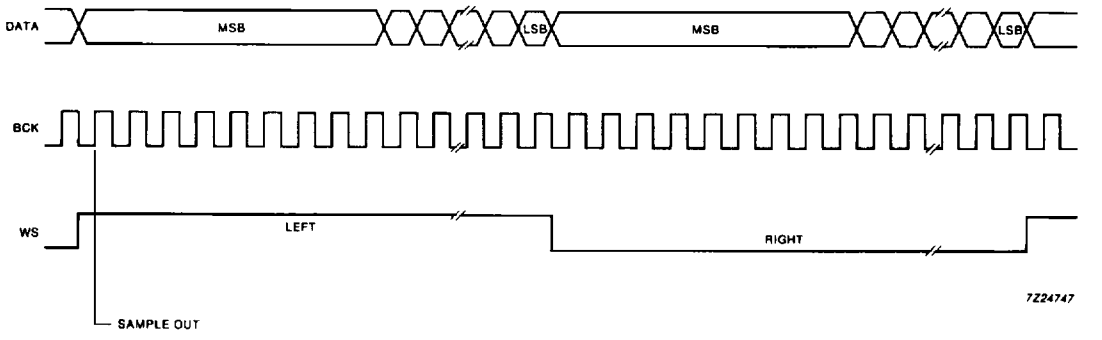


Fig.5 Format of input signals.